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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/916,555	07/26/2001	Chih Hsin Wang	2102397-911400	8544

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EXAMINER
PIZARRO CRESPO, MARCOS D

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 06/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/916,555	Applicant(s) WANG ET AL.	
	Examiner Marcos D. Pizarro-Crespo	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *27-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *27-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s) _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Attorney's Docket Number: 2101397-911400

Filing Date: 7/26/2001

Claimed Priority Dates: 4/26/2001 (Provisional 60/287,047)
3/12/2001 (Provisional 60/275,517)
1/5/2001 (Provisional 60/242,096)
9/20/2000 (Provisional 60/234,314)

Applicant(s): Wang et al.

Examiner: Marcos D. Pizarro-Crespo

DETAILED ACTION

This Office action responds to the amendment in paper no. 14 filed on 5/20/2003.

Acknowledgment

1. The amendment in paper no. 14, filed on 5/20/2003, in response to the Office action in paper no. 13, mailed on 3/24/2003, has been entered. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this Office action are claims 27-45.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 27-45 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee (US 6329685).

4. Regarding claim 27, Lee shows (see, *e.g.*, fig. 6I-4) all aspects of the instant invention including an electrically programmable and erasable memory device comprising:

- a substrate **10** of semiconductor material of a first conductivity type (p-type)
- first **30** and second **70** spaced-apart regions of a second conductivity type (n-type)
- a channel region between the first **30** and second **70** spaced-apart regions
- an floating gate **14** disposed vertically over and insulated from a portion of the channel region and a portion of the first region **30**
- an electrically conductive source region **50** electrically connected to the first region **30**, the source region **50** having:
  - a lower portion disposed vertically over the first region **30** and laterally adjacent to and insulated from the floating gate **14**
  - an upper portion that extends up and over the floating gate **14** and terminates in a first end that is vertically over and insulated from the floating gate **14**
- an electrically conductive control gate **40** having a first portion and a second portion

wherein:

- the first portion of the control gate **40** is laterally adjacent to and insulated from the floating gate **14**
- the second portion of the control gate **40** extends up and over the floating gate **14** and terminates in a second end that is vertically over and insulated from the floating gate **14**, and
- the first and second ends are laterally adjacent to and insulated from each other such that no portion of the control gate **40** is disposed directly between the floating gate **14** and the source region **50**

5. Regarding claims 28 and 32, Lee shows that the upper portion of the source-region **50** is wider than the lower portion of the source-region **50** (see, *e.g.*, fig. 6I-4).

6. Regarding claims 29 and 33, Lee shows the source region **50** having a substantially T-shaped cross-section (see, *e.g.*, fig. 6I-4).

7. Regarding claims 30, 35, 41, and 45, Lee shows the memory device further comprising an insulation layer **26** disposed directly between the floating gate(s) **14** and the second end(s), and a having a thickness permitting Fowler-Nordheim tunneling of charges therethrough (see, *e.g.*, col.8/ll.55-62).

8. Regarding claims 37, 38, 40, and 44, Lee shows the memory device further comprising insulation material **36** between the lower portion of the source region **50** and the floating gate(s) **14**, and having a thickness permitting voltage coupling therethrough (see, *e.g.*, col.12/ll.20-28). Lee also shows insulation material **36** directly between the first end(s) and the floating gate(s) **14**, and having a thickness permitting voltage-coupling therebetween (see, *e.g.*, col.12/ll.20-28).

9. Regarding claim 31, Lee shows (see, *e.g.*, fig. 6I-4) an array of electrically programmable and erasable memory devices comprising:

- a substrate **10** of semiconductor material of a first conductivity type (p-type)
- spaced-apart substantially-parallel isolation regions **20** formed on the substrate **10** and extending in a first direction (see, *e.g.*, fig. 2I-1)
- an active region between each pair of adjacent isolation regions **20**, each of the active regions including a column of pairs of memory cells extending in the first direction, each of the memory cell pairs including:
  - a first region **30** and a pair of second regions **70** spaced apart in the substrate **10** and of a second conductivity type (n-type)
  - channel regions formed in the substrate **10** between the first **30** and the second regions **70**
  - a pair of electrically conductive floating gates **14**, each disposed vertically over and insulated from a portion of the channel regions and a portion of the first region **30**
  - an electrically conductive source region **50** electrically connected to the first region **30**
  - a lower portion of the source region **50** that is disposed vertically over the first region **30** and laterally adjacent to and insulated from the pair of floating gates **14**
  - an upper portion of the source region **50** that extends up and over the floating gates **14** and terminates in a pair of first ends, each of the first

ends being disposed vertically over and insulated from one of the floating gates **14**

- a pair of electrically conductive control gates **40**, each having a first portion and a second portion

wherein for each of the control gates **40**:

- the first portion is laterally adjacent to and insulated from one of the floating gates **14**, and
- the second portion extends up and over one of the floating gates **14** and terminates in a second end that is disposed vertically over and insulated from the one of the floating gates **14**

and wherein each of the first ends is laterally adjacent to and insulated from one of the second ends such that no portion of the control gates **40** is disposed directly between the floating gates **14** and the source region **50**.

10. Regarding claims 34 and 43, Lee shows that the source regions **50** extend across the active regions and isolation regions **20** in a second direction substantially perpendicular to the first direction and intercepts one of the memory cell pairs in each of the active regions (see, *e.g.*, fig. 2I-1).

11. Regarding claim 36, Lee shows that the control gates **40** extend across the active regions and isolation regions **20** in a second direction substantially perpendicular to the first direction and intercepts one of the memory cell pairs in each of the active regions (see, *e.g.*, fig. 2I-1).

12. Regarding claim 39, Lee shows (see, *e.g.*, fig. 6I-4) all aspects of the instant invention including an electrically programmable and erasable memory device comprising:

- a substrate **10** of semiconductor material of a first conductivity type (p-type)
- first **30** and second **70** spaced-apart regions of a second conductivity type (n-type)
- a channel region between the first **30** and second **70** spaced-apart regions
- a floating gate **14** disposed vertically over and insulated from a portion of the channel region and a portion of the first region **30**
- an electrically conductive source region **50** electrically connected to the first region **30**, the source region **50** having:
  - a lower portion disposed vertically over the first region **30** and laterally adjacent to and insulated from the floating gate **14**
  - an upper portion that extends up and over the floating gate **14** and terminates in a first end that is disposed vertically over and insulated from the floating gate **14**
- an electrically conductive control gate **40** having a first portion and a second portion

wherein:

- the first portion of the control gate **40** is laterally adjacent to and insulated from the floating gate **14**, and

- the second portion of the control gate **40** extends up and over the floating gate **14** and terminates in a second end that is vertically over and insulated form the floating gate **14**
- the first and second ends are laterally adjacent to and insulated from each other such that there is no vertical overlap between the control gate **40** and the source region **50**

13. Regarding claim 42, Lee shows (see, *e.g.*, fig. 6I-4) all aspects of the instant invention including an array of electrically programmable and erasable memory devices comprising:

- a substrate **10** of semiconductor material of a first conductivity type (p-type)
- spaced apart isolation regions **20** formed on the substrate **10** to be substantially parallel to one another and extending in a first direction (see, *e.g.*, fig. 2I-1)
- an active region between each pair of adjacent isolation regions **20**, each of the active regions including a column of pairs of memory cells extending in the first direction, each of the memory cell pairs including:
  - a first region **30** and a pair of second regions **70** spaced apart in the substrate **10** and of a second conductivity type (n-type)
  - channel regions between the first region **30** and the second regions **70**
  - a pair of electrically conductive floating gates **14**, each disposed vertically over and insulated from a portion of one of the channel regions and a portion of the first region **30**

- an electrically conductive source region **50** electrically connected to the first region **30**, the source region **50** having:
  - a lower portion that is disposed vertically over the first region **30** and laterally adjacent to and insulated from the pair of floating gates **14**
  - an upper portion that extends up and over the floating gates **14** and terminates in a pair of first ends, each first end being disposed vertically over and insulated from one of the floating gates **14**
- a pair of electrically conductive control gates **40** each having a first portion and a second portion

wherein for each of the control gates **40**:

- the first portion is laterally adjacent to and insulated from one of the floating gates **14**, and
- the second portion extends up and over one of the floating gates **14** and terminates in a second end that is disposed vertically over and insulated from the one of the floating gates **14**

and wherein each of the first ends is laterally adjacent to and insulated from one of the second ends such that there is no vertical overlap between the control gates **40** and the source region **50**.

Response to Arguments

14. Applicant's arguments with respect to claims 27-45 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

15. The prior art made of record is considered pertinent to applicant's disclosure. Wang (US 5572054) describes the tunneling mechanism and operation of Lee's memory cell.

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

17. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

18. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Art Unit 2814 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(703) 308-7722** or **–7724**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Marcos D. Pizarro-Crespo** at **(703) 308-6558** and between the hours of 9:30 AM to 8:00 PM (Eastern Standard Time) Monday through Thursday or by e-mail via Marcos.Pizarro@uspto.gov If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on (703) 308-4918.

20. Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 308-0956**.

21. The following list is the Examiner's field of search for the present Office action:

Field of Search	Date
U.S. Class / Subclass(es): 257/314-326	6/16/2003
Other Documentation: PLUS Analysis	7/17/2002
Electronic Database(s): EAST (USPAT, EPO, JPO)	6/16/2003

LONG PHAM
PRIMARY EXAMINER

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MDP/mdp
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